Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 4, 6, 7, 19, 21, 22, 29, 31, 32, 39-47. Please amend claims 1, 5, 9, 10, 15, 16, 18, 20, 24, 26, 28, 30, 34, and 36, as follows:

Listing of Claims:

1. (Currently amended) A memory hub, comprising:

a local queue adapted to receive local memory responses, and operable to store the local memory responses;

a bypass path adapted to receive downstream memory responses, and operable to pass the downstream memory responses;

a buffered queue coupled to the bypass path and operable to store downstream memory responses;

a multiplexer coupled to the local queue, buffered queue and bypass path, the multiplexer being operable to output responses from ~~inform~~ a selected one of the queues or the bypass path responsive to a control signal; and

arbitration control logic coupled to the multiplexer, the arbitration logic operable to develop the control signal to control the selection of responses output by the multiplexer to alternately output a number of memory responses stored in the buffered queue and the same number of memory responses stored in the local queue if the number or a greater number of responses are stored in each queue.

2. (Original) The memory hub of claim 1 wherein the arbitration control logic develops the control signal to output memory responses stored in the local queue prior to memory responses stored in the buffered queue.

3. (Original) The memory hub of claim 1 wherein the arbitration control logic develops the control signal to output memory responses stored in the buffered queue prior to memory responses stored in the local queue.

4. (Cancelled)

5. (Currently amended) The memory hub of claim 1 [[4]] wherein the arbitration control logic assigns a time stamp to each memory request when the request is received by the hub~~, and wherein the age of each request corresponds to the assigned time stamp~~.

6. (Cancelled)

7. (Cancelled)

8. (Original) The memory hub of claim 1 wherein each of the local and downstream memory responses comprise data and a header identifying a memory request corresponding to the memory response.

9. (Currently amended) A memory hub adapted to receive local memory responses and downstream memory responses, the memory hub operable to store the received memory responses and operable to assign a time stamp to each memory request when the request is received by the memory hub and further operable to apply an arbitration algorithm to provide memory responses from local and buffered queues ~~select the order in which the stored local and downstream memory responses are provided~~ on an uplink output as a function of the age of a memory request associated with each memory response, the age of each request corresponding to the respective assigned time stamp.

10. (Currently amended) The memory hub of claim 9 wherein the memory hub <u>includes the</u> ~~further comprises a~~ local queue that stores the local memory responses and <u>the</u> [[a]] buffered queue that stores the downstream memory responses.

11. (Original) The memory hub of claim 10 wherein the memory hub further comprises a multiplexer coupled to the local queue, buffered queue, and bypass path, the multiplexer providing responses from one of the queues or bypass path on an output responsive to a control signal.

12. (Original) The memory hub of claim 11 wherein the memory hub further comprises arbitration logic coupled to the queues and the multiplexer, and wherein the arbitration logic applies the control signal to the multiplexer to control which memory responses are provided on the output.

13. (Original) The memory hub of claim 12 further including a bypass path coupled to the buffered queue and coupled to the multiplexer, the bypass path adapted to receive the downstream memory responses and operable to provide the responses to the multiplexer and the buffered queue.

14. (Original) The memory hub of claim 9 wherein each of the local and downstream memory responses comprise data and a header identifying a memory request corresponding to the memory response.

15. (Currently amended) A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the memory devices, the memory hub including,

a local queue adapted to receive local memory responses, and operable to store the local memory responses;

a bypass path adapted to receive downstream memory responses, and operable to pass the downstream memory responses;

a buffered queue coupled to the bypass path and operable to store downstream memory responses;

a multiplexer coupled to the local queue, buffered queue and bypass path, and operable to output responses from one of the queues or the bypass path responsive to a control signal; and

arbitration control logic coupled to the multiplexer, the arbitration logic operable to develop the control signal to control the selection of responses output by the multiplexer to alternately output a number of memory responses stored in the buffered queue and the same number of memory responses stored in the local queue if the number or a greater number of responses are stored in each queue.

16. (Currently amended) The memory module of claim 15 wherein each of the memory devices comprises ~~an SDRAM~~ a synchronous dynamic random access memory.

17. (Original) The memory module of claim 16 wherein the arbitration control logic develops the control signal to output memory responses stored in the local queue prior to memory responses stored in the buffered queue.

18. (Currently amended) The memory module of claim 16 [[17]] wherein the arbitration control logic develops the control signal to output memory responses stored in the buffered queue prior to memory responses stored in the local queue.

19. (Cancelled)

20. (Currently amended) The memory module of claim 15 [[19]] wherein the arbitration control logic assigns a time stamp to each memory request when the request is received by the hub~~, and wherein the age of each request corresponds to the assigned time stamp~~.

21. (Cancelled)

22. (Cancelled)

23. (Original) The memory module of claim 15 wherein each of the local and downstream memory responses comprise data and a header identifying a memory request corresponding to the memory response.

24. (Currently amended) A memory system, comprising:

a memory hub controller;

a plurality of memory modules, each memory module being coupled to adjacent memory modules through respective high-speed links, at least one of the memory modules being coupled to the memory hub controller through a respective high-speed link, and each memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the memory devices, the memory hub comprising,

a local queue adapted to receive local memory responses, and operable to store the local memory responses;

a bypass path adapted to receive downstream memory responses, and operable to pass the downstream memory responses;

a buffered queue coupled to the bypass path and operable to store downstream memory responses;

a multiplexer coupled to the local queue, the buffered queue and the bypass path, and operable to output responses from one of the queues or the bypass path responsive to a control signal; and

arbitration control logic coupled to the multiplexer, the arbitration logic operable to develop the control signal to control the selection of responses output by the

multiplexer to alternately output a number of memory responses stored in the buffered queue and the same number of memory responses stored in the local queue if the number or a greater number of responses are stored in each queue.

25. (Original) The memory system of claim 24 wherein each of the high-speed links comprises an optical communications link.

26. (Currently amended) The memory system of claim 24 wherein at least some of the memory devices comprise ~~SDRAMs~~ synchronous dynamic random access memories.

27. (Original) The memory system of claim 24 wherein the arbitration control logic develops the control signal to output memory responses stored in the local queue prior to memory responses stored in the buffered queue.

28. (Currently amended) The memory system of claim 24 [[27]] wherein the arbitration control logic develops the control signal to output memory responses stored in the buffered queue prior to memory responses stored in the local queue.

29. (Cancelled)

30. (Currently amended) The memory system of claim 29 wherein the arbitration control logic assigns a time stamp to each memory request when the request is received by the hub~~, and wherein the age of each request corresponds to the assigned time stamp~~.

31. (Cancelled)

32. (Cancelled)

33. (Original) The memory system of claim 24 wherein each of the local and downstream memory responses comprise data and a header identifying a memory request corresponding to the memory response.

34. (Currently amended) A computer system, comprising:

a processor;

a system controller coupled to the processor, the system controller including a memory hub controller;

an input device coupled to the processor through the system controller;

an output device coupled to the processor through the system controller;

a storage device coupled to the processor through the system controller;

a plurality of memory modules, each memory module being coupled to adjacent memory modules through respective high-speed links, at least one of the memory modules being coupled to the memory hub controller through a respective high-speed link, and each memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the memory devices and coupled to the corresponding high-speed links, the memory hub including,

a local queue adapted to receive local memory responses, and operable to store the local memory responses;

a bypass path adapted to receive downstream memory responses, and operable to pass the downstream memory responses;

a buffered queue coupled to the bypass path and operable to store downstream memory responses;

a multiplexer coupled to the local queue, the buffered queue and the bypass path, and operable to output responses from a selected one of the queues or the bypass path responsive to a control signal; and

arbitration control logic coupled to the multiplexer, the arbitration logic operable to develop the control signal to control the selection of responses output by the multiplexer to alternately output a number of memory responses stored in the buffered queue and the same number of memory responses stored in the local queue if the number or a greater number of responses are stored in each queue.

35. (Original) The computer system of claim 34 wherein each of the high-speed links comprises an optical communications link.

36. (Currently amended) The computer system of claim 34 wherein at least some of the memory devices comprise ~~SDRAMs~~ synchronous dynamic random access memories.

37. (Original) The computer system of claim 34 wherein the processor comprises a central processing unit (CPU).

38. (Original) The computer system of claim 34 wherein each of the local and downstream memory responses comprise data and a header identifying a memory request corresponding to the memory response.

39-47. (Cancelled)